SuperComputers For Space Applications

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Abstract

The goal of this paper is to give the ALCATEL SPACE (ASP) vision on the way the COTS based computer could be introduced in Space systems. This paper will first present the ASP's experience acquired on COTS processors since the Skybridge project up to now. It will depict how it has been reused for the GAIA project. Finally, extending the technologies used in the frame of GAIA, it will provide a quick overview of the potential impacts for the next generation space products.

1. INTRODUCTION

Upcoming new science and Earth observation projects, like GAIA, make the need for high computing power systems more and more evident in the Space community. Commercial technologies, like PowerPC processors, have very promising properties, one of them being obviously the computing performance, but not only. The new micro–electronic technologies (0,09μ) used for Ground applications are about to face very similar environmental failures that the ones specific to the Space environment. Tests performed by Space agencies (ESA & CNES) in order to verify the SEU tolerance of such technologies and the results obtained, allow us to imagine a possible convergence between the Space & Ground technologies in order to be able to use "Supercomputers" for space applications. Those Supercomputers, associated with fault tolerance techniques, could be used to complement the European rad-hard LEON processors line. They would allow us to address innovative solutions for next generation of computing systems for scientific high processing power payload computers as a first step. Then, once the validity of this technology has been demonstrated, one can imagine the revolution it will generate in Space systems.

In the following paragraphs, we will first depict the work performed by ASP and the experience acquired on COTS processors associated with fault tolerance techniques. It will depict how it has been reused for the GAIA project. And finally it will provide an overview

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of the potential impacts for the next generation space products families from high reliability to high availability (in terms of cost reduction, design risk reduction, flexibility, hardware and software reusability, building blocks standardisation, etc…).

2. ALCATEL SPACE EXPERIENCE IN FAULT TOLERANCE ACTIVITIES

2.1 SKYBRDIGE, AS THE STARTING POINT

ASP started Fault tolerance activities on COTS in 1998, with the help of the CNES in the context of the Skybridge studies. This project was designed to provide a space network based on a constellation of 64 low orbit satellites, in order to provide fast internet access, with multimedia services (like interactive video, games, etc…). Here below is given an illustration of the space segment of the network .

__Figure 1 : Picture of the Skybridge network space segment__

As one can imagine, the computing power required for the payload software was important as several complex functions had to be managed by the payload directly (antenna pointing management, multi-spot management, mission plan management, etc…). Also, there was an important number of payloads equipments to produce. So, we decided to start a study in order to prepare a new generation of computer board , in order to complement the existing rad-hard space processors.

The main objectives of this Fault tolerance study were :
- To develop a new generation powerful building block processor board matching the high computing performance requirements for scientific and telecom payloads (Ex : Payload Management Unit of Skybridge, On Board communication Processors),
- To define new generation software development facilities based for example on automatic code generation concepts.

2.2 ABSTRACT OF THE WORK PERFORMED

We identified the PowerPC processor as a good COTS component that can be used to implement fault tolerance techniques. Indeed, this microprocessor has a good behaviour against radiations, and is latch-up free by design (SOI technology). It is also the one that has the best CPU computing power / power consumption ratio (ex: PowerPC603e ➜ 80 Mips for 2 Watts, and more recently the PowerPC750 / 800 Mhz ➜ 1800 Mips for 4 watts).

A 603^e PowerPC board has been developed by the CNES and delivered to us to build the first Fault Tolerance architecture (so called "DMT"=Duplex Multiplexed in Time) imagined by the CNES. This first release was relying on hardware protection mechanisms and for a large part, on software control . Here below is given a picture of the board developed to build the architecture , and on the right a copy of the software static architecture.
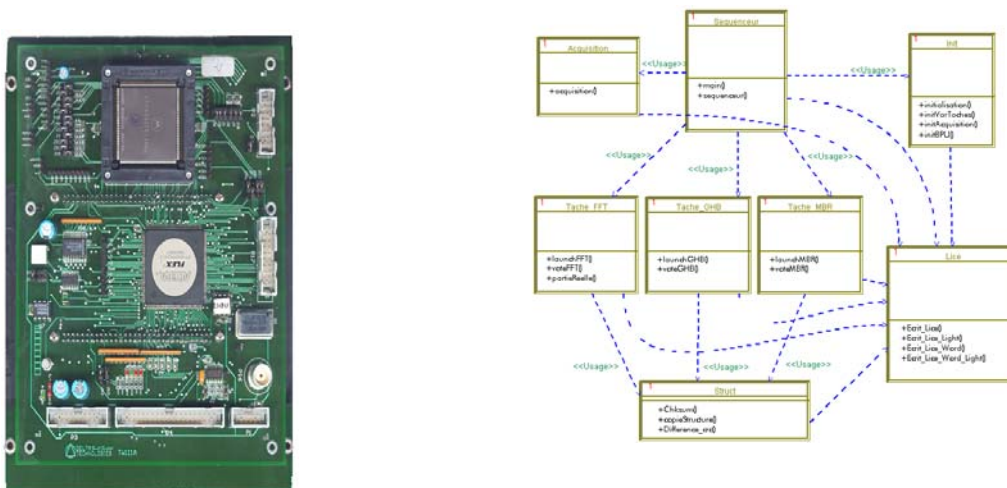
Figure 2 : PowerPC board developed and Software Static architecture

The software was based on a Micro-scheduler that was responsible in scheduling three tasks implementing typical payload software processing (Acquisition of Data, Signal Processing and TM production) at a period around 10 Millisecond. This scheduler was responsible in implementing the DMT™ Fault tolerance technique.

In the *Figure 3* is depicted a typical Real time processing cycle as implemented in the First version of the DMT. The principle was quite simple, each real time cycle, each task performed acquisition processing and voting of the results. The protection of the acquired and produced data was guaranteed by a specific hardware implementation.
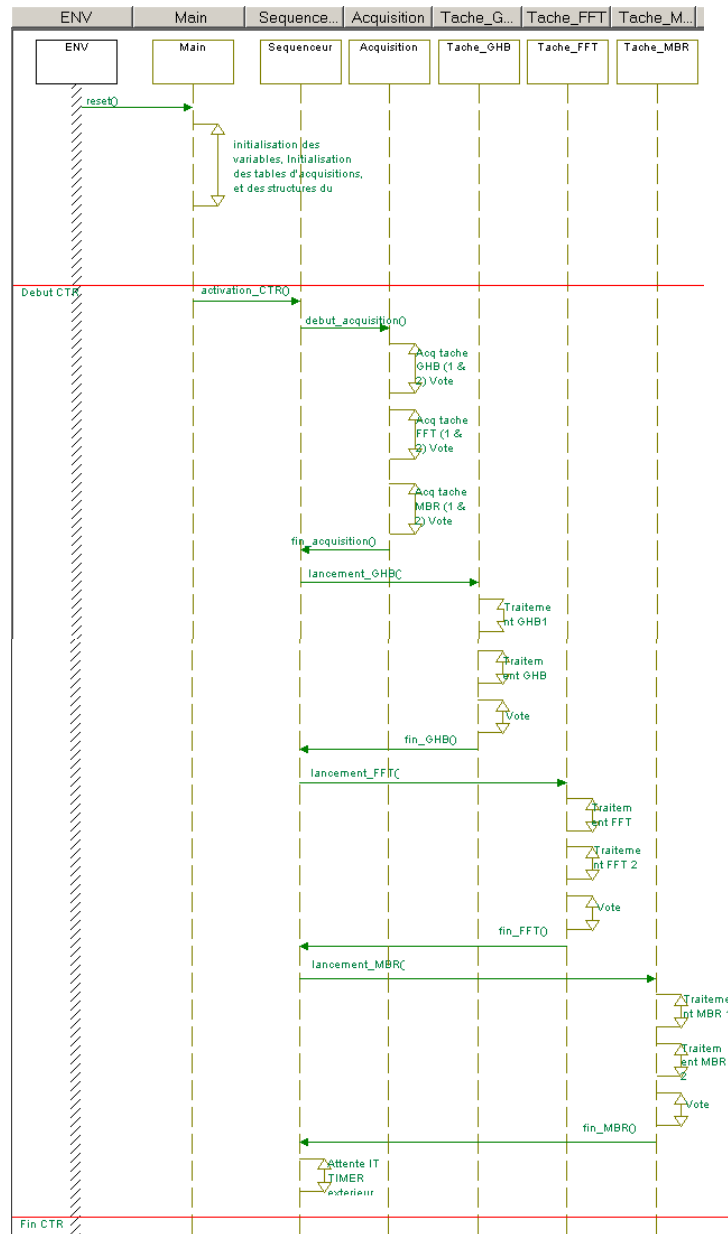
Figure 3 : Illustration of a typical Real Time processing cycle

Once this architecture has been developed, several tests campaign at DERTS and IPN have been performed in order to measure the reliability of the software and hardware when exposed to radiations. The tests performed demonstrated very good results in term of reliability and error detection and recovery in case of SEU. (95% of the failure have been detected and recovered from the Software).

However, as the DMT technique was very restricting for software development and CPU consuming, some improvements have been defined at hardware level in order to suppress some constraints at Software level : It was the DT2 concept.

The DT2 has been designed in order to make the Fault tolerance management transparent to software developers. In this architecture the Fault tolerance management was now managed at macro cycle level by a dedicated hardware (ASIC, FPGA) responsible to control the data fluxes in input and output of the two processors running in parallel.

In the *Figure 4* is depicted the general architecture of the DT2 concept :

Processing Unit Core with DT2

Other parts of the computer
(Backplane bus - I/O bus)
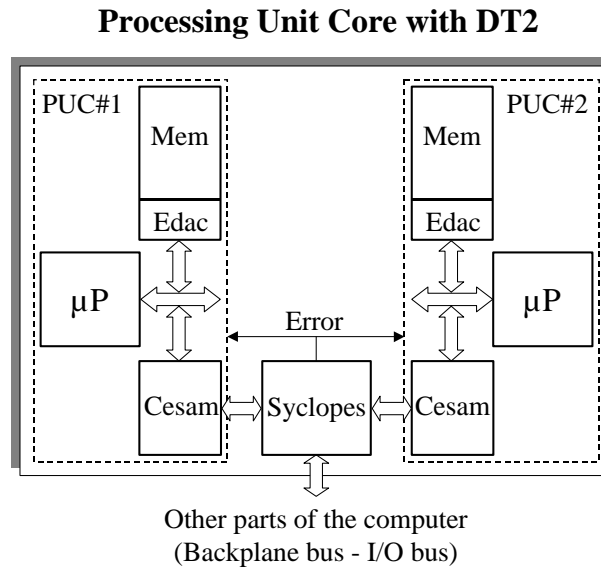
Figure 4 : DT2 General architecture

2.3 OTHERS AVAILABLE COMMERCIAL SOLUTIONS

In parallel with the work performed with the CNES, US companies have also worked on this topic, in particular Maxwell Technologies with new generation processors like PowerPC. This company has developed a triplicated and micro-synchronised PowerPC board based on three PowerPC 750FX. This board is TMR ("Triple Modular Redundancy") protected, as depicted below, in the *Figure 5*. The three processors are controlled and voted by a dedicated SEU immune FPGA. This FPGA realises the interface between the processors and the rest of the world (memories, interface buses, etc…). This board has been evaluated in the frame of the Gaïa project, and no problem has been found using it.

It has very interesting properties because it offers a CPU power of 1500 Mips, and the development of a software is fully transparent with regard to the Fault tolerance management. All these stuff are provided and encapsulated inside the provided BSP ready for use.
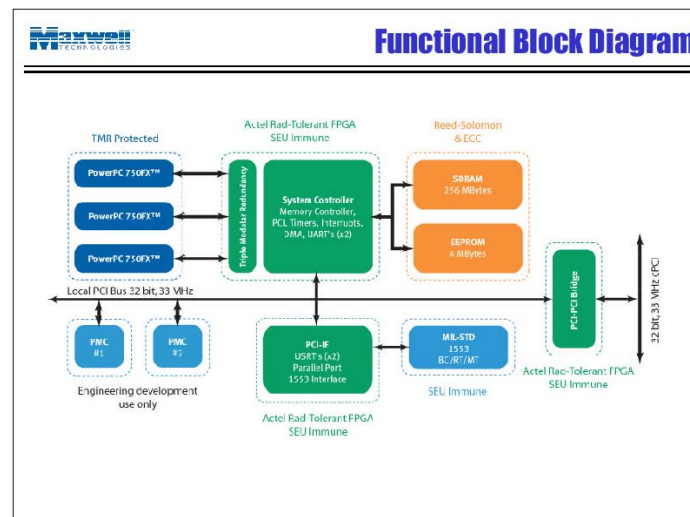
Figure 5 : General Architecture of the Maxwell board

The mains drawbacks of this kind of board is first the power consumption that is three times higher than a single processor module. And also, the resynchronisation period during which the system is not operational (~1 millisecond.). This last point can be managed, and must be taken into account at project level, as the resynchronisation period can be programmed by software, it must be defined according to the mission reliability constraints analysis.

Radiations tests performed by NASA/JPL has demonstrated that this board is very reliable, and that it can be used for space applications. The best example is that Maxwell Technologies announced recently that Northrop Grumman Space Technology (NGST) has selected Maxwell's SCS750 single board computer (SBC) for spacecraft control and payload data management for the National Polar-orbiting Operational Environmental Satellite System (NPOESS).

3. REUSE OF THE EXPERIENCE IN THE FRAME OF GAIA

3.1 GAÏA IN A FEW WORDS

Gaia is a global space astrometry mission. Its goal is to make the largest, most precise map of our Galaxy by surveying an unprecedented number of stars - more than a thousand million. Gaia is a mission that will conduct a census of one thousand million stars in our Galaxy. It will monitor each of its target stars about 100 times over a five-year period, precisely charting their distances, movements, and changes in brightness. It is expected to discover hundreds of thousands of new celestial objects, such as extrasolar planets and failed stars called brown dwarfs. Within our own Solar System, Gaia should also identify tens of thousands of asteroids.

Mission specification :
- Scheduled for launch :   2010
- Operational period :   5 years
- Availability in orbit : > 95 %
- Altitude :   L2 orbit

Figure 6 : Gaia mapping the stars of the Milky Way

More about the project can be found on the ESA web site.

3.2 THE ACTIVITIES IN THE FRAME OF GAÏA

One of the major difficulties of this challenging project is situated at the payload level (VPU : Video Processing Unit) responsible of the star detection algorithm execution.

The experience acquired in developing software for PowerPC COTS based computer and all the software development facilities (in particular based on automatic code generation from UML design) have been of a great interest for the Gaïa project and reused directly in the frame of the benchmarking activities.

Here below is given a picture of the simple development facilities reused from Skybridge in order to test detection algorithm with a VPU simulator based on a the new Maxwell Super Computer .
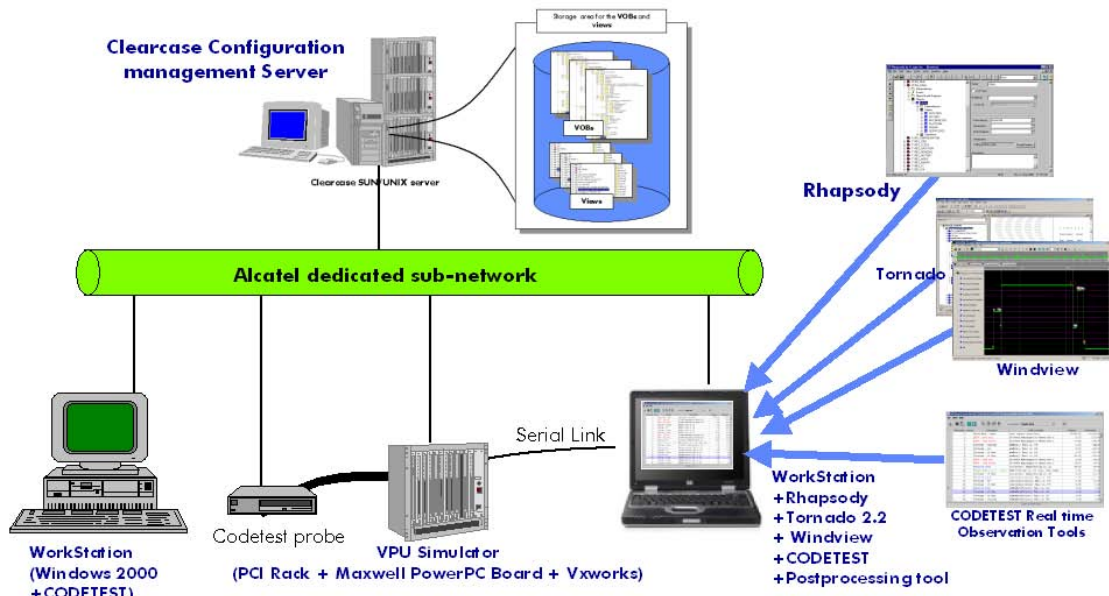
Figure 7 : General Architecture the test facilities with Super Computer

Having all the development facilities quickly operational allowed us to focus on the Gaïa application difficulty which is the star detection algorithm, with specific point of interest in the pure algorithm execution time according to several configuration that had to be verified. Those points were directly linked to the fact that we were using Supercomputers with Instruction and Data caches L1 and L2 for example. But also, due to the fact that TMR management had to be tested and configured in order to verify the behaviour of the software in case of error injection (in particular during a resynchronisation).

The test performed during the Gaïa Phase A activities, demonstrated that the image processing should be realised by software for in flight flexibility and maintainability reasons. And in this case, a computing power of around 700 Mips would be required to process acquisition channels.

4. TODAY CURRENT SITUATION

Today, even if the computing power of the rad-hard space processors has increased seriously since several years, it is still not enough to cover particular payload scientific mission like Gaïa.

In a few years, we came from the 1750 processor with a computing power of less than 1 Mips, to the DSP21020 and ERC32 with a computing power of around 14 Mips. The next generation for European rad-hard space processor is the LEON which will offer a power around 100 Mips. This processor is today available in Alpha test version at Alcatel Space for evaluation, and will be available beginning 2006 in Flight Model.

This new generation processor will allow to cover widely more applications, allowing to add more software processing on board (replacing some hardware functions by a software implementation for example).

However, even with a LEON processor, particular scientific missions will not be able to be developed if a part of the processing is not implemented in hardware (ASIC or FPGA).

In parallel with the rad-hard processor roadmap, new commercial COTS based SuperComputer boards will be soon available in flight model.

These new emerging products show us that to cover all space missions needs we have now two possible ways :

- "Classical" radiation hardened computers :
    - Based on single rad-hard processor
    - But "limited" in computing power

- "Commercial Based" Super Computers :
    - Associated with Fault tolerance techniques (DMT, DT2, TMR or TTMR,…)
    - At least 50 times faster than a rad-hard processor (depending on the type of processing)

Obviously the first one must be the baseline for the European space community, but in order to be cover special need the COTS based Super Computers way must also be investigated as a complement to the baseline.

In the *Figure 8* below, is depicted the evolution of the CPU power up to today and the possible tandem for the future.
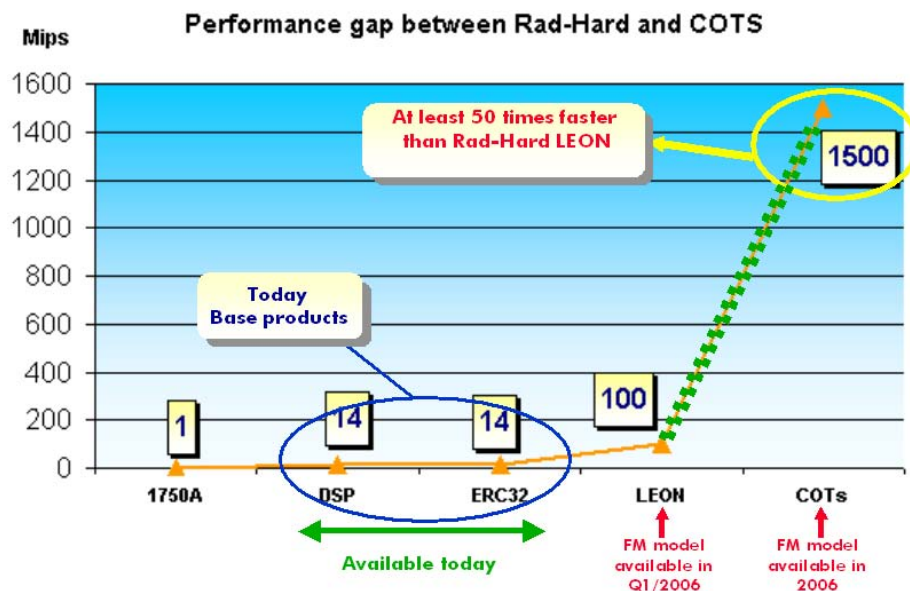
Figure 8 : Supercomputers as a complement to rad-hard baseline roadmap for specific applications

4.1 POSSIBLE IMPACT OF THE COTS ON THE SPACE PRODUCTS.

Today it is the first time that a project (Gaïa) is demonstrating the need of computing power on board payload. We can easily imagine that it is not the last, it would not be in the logic of the history. Other project needing high-bandwidth data processing and algorithmic intensive computing with flexibility on board will arrive (like on-board telecom network switching for example).

Trying to imagine what we could do with this kind of technology onboard is an easy exercise. For example, we could go a step further from the current building block approach, by simplifying payload equipment architecture by creating a "multi-mission" payload building block based on a generic HW architecture and a software that could be tailored from a mission to another. We could earn in flexibility, by reducing the fixed design costs, by reducing the risk of redesigning HW, etc… In terms of deployment, we could first build "High-reliable" Super Computers (the first would be the Gaïa VPU) that could accept some outages. Then, once the technology has been demonstrated in flight, we could go up to "High available" computers.

5. CONCLUSION

As it is evident that the European new rad-hard LEON processor roadmap must stay the baseline, it is also important to continue investigate the way of the COTS based Super Computers. Some Us commercial solutions are already available for Flight missions (Ex :NPOESS). And as anyone knows, those innovative solutions are rarely ITAR free, so it seems important to investigate this way at European level, by building a common project in order to have an equivalent Super Computer solution in case the ITAR constraint is verified. Several companies in Europe (SMEs and primes) have already a strong experience in this domain, a good idea would be to work together with the help of Space agencies.

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